REMARKS

Claims 1-24 are pending in the present application. Claims 1, 8, 13 and 18 have been amended herein. No new matter has been added. Applicants respectfully request reconsideration of the claims in view of the following remarks.

Applicant notes with appreciation the allowance of claims 11 and 12.

Claims 1-8 and 13-16 have been rejected under 35 U.S.C. § 102(a) as being anticipated by Lakhani and claims 9-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Lakhani in view of Zer. Applicant respectfully traverses these rejections.

Claim 1, as previously presented, specifically recites that "the remaining bits provide a byte address when the address argument is a byte address argument and the remaining bits provide a block address when the address argument is a block address argument." The claim has been amended herein to further recite that "the block address [has] the same number of bits as the byte address." Applicant respectfully submits that the references of record do not teach or suggest the limitations of claim 1.

In Lakhani, contrary to the claimed invention, the address argument bits are always either block address bits or byte address bits. In particular, address bits A22:A19 determine the main block and address bits A18:A16 determine the erase block. Lakhani, Par. [0038]. Further, address bits A4:A0 determine the byte. *Id.* This addressing scheme remains in all modes. *See* Lakhani, Par. [0069]-[0070]. There are no two modes where particular bits (i.e., the "remaining bits" in claim 1) provide a byte address in one mode and a block address in the other mode. In each case the address bits A22:A19 point to the same place in memory.

The Examiner correctly points out that address field A[22:0] comprise high order bits such as A[22:A19], which represent a larger block range of addresses and low order bits such as

A[4:0], which represent a smaller range of addresses, and bit A[0], which represents the lowest address bit. Applicant agrees but notes that the lower order bits are never used in any block mode taught by Lakhani. To clarify this point, the claims have been specifically amended to recite that the block address has the same number of bits as the byte address. As noted by the Examiner, Lakhani teaches a mode where each set of address bits A(22:0) and AX is associated with a data byte. Par. [0069]. Lakhani, however, never teaches a 24-bit block address.

In the claimed invention, on the other hand, the remaining bits, however many there are, provide a byte address when the address argument is a byte address argument and the remaining bits provide a block address when the address argument is a block address argument. This scheme is simply not taught or suggested by the prior art.

Claims 2-7 depend from claim 1 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claim 8, as amended, specifically recites that "in the byte addressing mode, address bits of an address argument of the command provide a byte address, and in the block addressing mode, said address bits of the address argument of the command provide a block address, the block address having the same number of bits as the byte address." As discussed above with respect to claim 1, the prior art of record never teaches or suggests a number of address bits that provide a byte address in a first mode and a block address in a second mode. Therefore, it is respectfully submitted that claim 8 is allowable over the references of record.

Claims 9-10 and 17 depend from claim 8 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claim 13, as amended, specifically recites "when said address argument is a byte address argument, address bits of the address argument provide a byte address, and when said address argument is a block address argument, said address bits of the address argument provide a block address, the block address having the same number of bits as the byte address." As discussed above with respect to claim 1, the prior art of record never teaches or suggests a number of address bits that provide a byte address in a first mode and a block address in a second mode. Therefore, it is respectfully submitted that claim 13 is allowable over the references of record.

Claims 14-16 depend from claim 13 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claim 18, as amended, specifically recites "receiving a command that includes an address argument comprising a plurality of address bits and an addressing mode field, the addressing mode field indicating whether the address argument contains a byte address or a block address, the block address and the byte address having the same number of bits." As discussed above with respect to claim 1, the prior art of record never teaches or suggests a number of address bits that provide a byte address in a first mode and a block address in a second mode. Therefore, it is respectfully submitted that claim 18 is allowable over the references of record.

Claims 19-24 depend from claim 17 and add further limitations. It is respectfully submitted that these claims are allowable over the references of record in view of their dependence on an allowable claim as well as the additional limitations.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Ira S. Matsil, Applicant's attorney, at 972-732-1001, so that such issues may be resolved as expeditiously as possible. If the enclosed fees are deemed to be insufficient, the Commissioner is hereby authorized to charge, or credit any overpayment to, Deposit Account No. 50-1065.

Respectfully submitted,

/Ira S. Matsil/

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